AUTUMN END SEMESTER EXAMINATION-2015

5th Semester B. Tech & B. Tech Dual Degree

CO&A (CS-3005)/ CS&A (CS-505)

SOLUTION SCHEME

1. Short Questions

Speed of processor is 8 MHz.

Cycle Time=1/(8×106 )

ALU Operation =50%

Memory Operation =30%

Branch Operation=20%

Total Time=(1/(8×106 ))×(50%×4+30%×9+20%×7)=7625×10-6

[1000]=J

[1004]=S

1. A+B+2

|  |  |
| --- | --- |
| **I/O mapped I/O** | **Memory mapped I/O** |
| Memory and I/O devices will be addressed by the same address. | Memory and I/O can't have same address. |
| Total number of memory and I/O devices will be less in number. | Total number of memory and I/O devices are more as they use all address space. |

1. Nested sub-routine.

|  |  |  |
| --- | --- | --- |
| 8-bits (Op-code) | 6-bits (Reg-addr) | 18-bits (Mem-addr) |

<---------------------------------------------32 bits------------------------------------->

Size of Memory is: 218 words=256K words.

1. 128k×16=217 ×16

Required is 4M×32=222 ×2×16=223 ×16

223 ×16=2X ×217 ×16

x=6, 26 = 64

1. Block size=16 bytes.

No. of blocks in the cache=(128×1024)/16=213

No. of sets=213 /4=211

SIMD: Single Instruction Stream Multiple Data Stream.

MIMD: Multiple Instruction Stream Multiple Data Stream.

M=010, M'+1=110

A Q Qn+1  SC

Initialization 000 101 0 011

SUB M 110 101 0

AShiftR 111 010 1 010

ADD M 001 010 1

AShiftR 000 101 0 001

SUB M 110 101 0

AShiftR 111 010 1 000

So, Product=AQ=111010

1. Virtual memory is a technique that allows the execution of processes which are not completely available in memory. The main visible advantage of this scheme is that programs can be larger than physical memory. Virtual memory is the separation of user logical memory from physical memory.

figure5

* **Address Translation Mechanism:**All programs and data are composed of fixed-length units called pages, each of which consists of a block of words that occupy contiguous locations in the main memory. Page cannot be too small or too large. The virtual memory mechanism bridges the size and speed gaps between the main memory and secondary storage. The page table information is used by the MMU for every access, so it is supposed to be with the MMU. However, since MMU is on the processor chip and the page table is rather large, only small portion of it, which consists of the page table entries that correspond to the most recently accessed pages, can be accommodated within the MMU.

|  |  |  |
| --- | --- | --- |
| 10-bits (Op-code) | 7-bits (Reg-addr) | 28-bits (Mem-addr) |

<---------------------------------------------45 bits------------------------------------->

Operations: 210

One address memory operations: (210-450) ×228

1. **Programmed I/O**:Once the data is initiated the CPU starts monitoring the interface to see when next transfer can made. The instructions of the program keep close tabs on everything that takes place in the interface unit and the I/O devices. In this technique CPU is responsible for executing data from the memory for output and storing data in memory for executing of Programmed I/O.

**Drawback of the Programmed I/O**:The main drawback of the Program Initiated I/O was that the CPU has to monitor the units all the times when the program is executing. Thus the CPU stays in a program loop until the I/O unit indicates that it is ready for data transfer. This is a time consuming process and the CPU time is wasted a lot in keeping an eye to the executing of program. To remove this problem an Interrupt facility and special commands are used.

**Hazard**: Stall in pipeline.

**Types of hazard**

(i) Data Hazard

(ii) Structural Hazard

(iii) Control Hazard

**Solutions of Data Hazard**

(i) Operand forwarding.

(ii) By s/w (NOP)

(iii)Reordering the instructions.

Direct: 900

Immediate:601

Relative:1502

Register Indirect:100

Index: 1000

14.25=1110.01

Normalized value=1.11001×23

E ' = 3+127=130=10000010

M=110010 . . . 0

S=0

**Special Values:**

|  |  |  |
| --- | --- | --- |
|  | **E'** | **M** |
| **0** | 0 | 0 |
| **∞** | 255 | 0 |
| **NaN** | 255 | ≠0 |
| **Denormal Number** | 0 | ≠0 |

Control Steps of ADD R1, (R2)

1. PC out, MAR in, Read, Select 4,Add,, Z in

2. Z out, PC in , Y in ,WMFC

3. MDRout , IR in

4. R2out , MARin , Read

5. R1out, Y in , WMFC

6. MDRout , Select Y, ADD, Z in

7. Z out, MDR in

8. R2out , MARin , Write

9. WMFC, End.

Micro routine of ADD R1, (R2)

1. In microprogrammed control unit , the logic of the control unit is specified by a microprogram. A microprogram consists of a sequence of instructions in a microprogramming language. These are the instructions that specify microoperations. Microprogram are stored in microprogram memory and the execution is controlled by microprogram counter (PC ) .Microprogram consists of microinstructions which are nothing but the strings of 0’s and 1’s .

figure7

(i) Micro Instruction

(ii) Micro Routine

(iii) Micro Program Counter

(iv) Control Store

1. **Content-addressable memory** (**CAM**) is a special type of computer memory used in certain very-high-speed searching applications. It compares input search data (tag) against a table of stored data, and returns the address of matching data.



The key register holds a mask that allows searching based on part of argument. If a bit in the key register is 1, then the corresponding bit in the argument and each memory word must be the same to be considered a match. If a bit in the key register is 0, then the corresponding bit is considered a match whether or not the argument and memory word are equal for that bit. This allows searches for words where any subset of the bits match the argument register.

**Match Logic:**

The match register, M, is m bits wide and will contain a 1 for each word that matches the masked argument, and a 0 for each word that does not.

Bit j in word i (Fi,j) is considered a match for bit j in the argument (Aj) if they are the same, or if bit j in the key (Kj) is zero, indicating that we don't care about it.

Mi = (Fi,jAj) + (F'i,jA'j) + K'j for all j = 1 to n



**How it is different from RAM?**

1. Associative memory unit is accessed by content but RAM is accessed by address.

2. An associative memory is more expensive than RAM because each cell must have storage capacity as well as logic circuit for matching its content with an external argument.

3. Associative memory is used in applications where the search time is very critical and must be very short.

(i)

h1=0.7

Tavg1=50ns

Tavg2=Tavg1+20% of 50=50+10=60ns

t1=t2/10

Tavg=0.7×t1 + 0.3 × (10×t1)

t1=13.51ns

t2=10×t1=135.1ns

(ii) Tavg2=hN × t1+(1- hN ) × t2

60= hN ×13.51+ (1- hN ) × 135.1

hN = 0.61

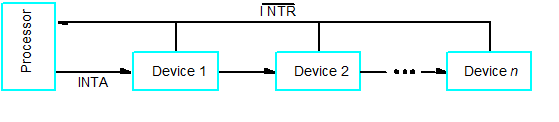
(iii) Change in hit ratio is=0.7 - 0.61= 0.09

Percentage of change in hit ratio=0.09/0.7×100= 12.85%

**Vectored Interrupt**: A device requesting an interrupt can identify itself by sending a special code to the processor over the bus.

**Daisy chain**

Simultaneous arrivals of interrupt requests from two or more devices. The processor must have some means of deciding which request to service first.



Pipeline Stages Stage Delay(ns) Overhead(ns) Tclk

A 9 2 1 : 3ns

B 5 2, 4, 3, 2, 2 1 : 5ns

TA = (9+99)×3ns=324ns

TB = (5+99) ×5ns=520ns

Time saved=520-324=196ns

1. Cycle Stealing Vs Burst Mode

|  |  |
| --- | --- |
| **Cycle Stealing of DMA** | **Burst Mode of DMA** |
| It is the data transfer technique in which one data word is transferred and then control is returned to CPU. | It is the DMA data transfer technique in which number of data words are transferred continuously until whole data is not transferred. |
| Data is transferred only when CPU is idle. | Data transfer continues until whole data is not transferred. |
| It is slow data transfer technique. | It is very fast data transfer technique. |
| High CPU utilization because data is transferred when CPU has no task to perform. | Low CPU utilization because CPU remains idle until whole data is not transferred. |
| Extra overhead because every time CPU has to be monitored for idle periods or slots. | No need to check CPU idleness. |

1. RISC Vs CISC

|  |  |
| --- | --- |
| **RISC** | **CISC** |
| Processors with simple instructions are called Reduced instruction set computers. | Processors with complex instructions are called complex instruction set computers. |
| Single clock cycle. | Multiple clock cycles. |
| Emphasis on software. | Emphasis on hardware. |
| Large code size. | Small code size. |
| Simple addressing modes. | Complex addressing modes. |
| Large number of registers are used. | Small number of registers are used. |